Fabrication of Field Effect Transistor based on Graphene Sheet

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ABSTRACT

We fabricated bipolar field-effect transistors based on graphene and analyzed their performance. A field effect transistor includes a P-type semiconductor substrate as a back gate, graphene sheet is used as the channel material in device with transferring graphene sheet from Cu substrates to target substrates, source and drain electrodes formed at a distance 6 μm, and junctions between the source and drain electrodes and the semiconductor region are formed as an insulated area including a schottky barrier. When the device was tested at room temperature, it exhibited V-shaped ambipolar transport properties with the minimum conductivity at around VGS ~ 1V, charge neutrality point (CNP) where the electrons and holes are equal in density, from p-type region to n-type region. This research investigared the preparation of back gate field effect transistor with graphene sheet via a low-cost manufacturing method. The reasults suggest that our method is fast, facile, and substrate independent.
Keyword: Field effect transistor, electrode, graphene, bipolar.

Introduction

Carbon has various crystalline allotropes such as diamond, graphite, graphene and nanotubes. The carbon atoms in diamond are sp^3 hybridized and sp^2 hybridized in the rest of them. Graphene is a two-dimensional network of carbon atoms arranged on a honeycomb lattice. A stack of graphene sheets bound by weak van der Waals forces is graphite. A graphene sheet rolled into a tube is a carbon nanotube (CNT). A graphene sheet with at least 12 pentagonal defects results in fullerene. Graphene was not known to exist in isolated form until 2004 when it was first isolated by Novoselov's group in Manchester [1]. Devices base on graphene, provides a variety of novel applications such as field-effect transistors (FETs) [2] , ultrasensitive sensors [3], transparent electrodes, sensors due to its large detection area, and novel nan composites [4]. Despite of the promising electronic properties, graphene field effect transistor cannot at present utilized in digital logic since graphene does

not have a band gap in its natural state and cannot completely block the current in the transistor's off-sate. Graphene with its exceptional electronic properties can be a possible alternative for silicon. Although CNTs which offer similar electronic properties have been considered as a replacement for silicon, the fact that graphene with its planar geometry can be processed with more conventional complementary metal oxide semiconductor (CMOS) technology gives it a significant advantage over CNTs. However, a major drawback for such use of bulk graphene is its zero band gaps, which makes the graphene based FETs hard to switch off. The purpose of this research was to study the behavior of graphene in field effect transistor. Therefore, a planar sheet of high quality graphene as a channel was essential for the field effect transistor. In section 2 after creating markers on the insulation substrate, graphene based devices (two electrode, multiple electrodes and back gated field effect transistors) were fabricated using photolithography and lift-off processes. In section 3, after the transfer of graphene sheet to desired substrate, Raman spectroscopy was used to analyze the quality of graphene and fabrication of the S/D electrodes. In section 4, simulation of the Transmission spectrum of graphene nanoribbon is done and ends with the conclusion.

Fabricating transistor

To fabricate an FET, p-type 100 wafer with a thickness of 400 micrometer available in the laboratory with 30 ohm/cm resistance properties were used. Wafers are cut in dimensions of 1.45 1.45 cm. To clean the samples, we use the RCA method, two parts of H_2o, two parts of NH_4OH and two parts of H_2o_2 solution. The provided solution was heated at 80 5°C and samples were submerged in it for 15 min. Then, the samples were washed in a container containing deionized water for 10 min at ambient temperature. Finally, the samples were exposed to wind and were cleaned. For oxide deposition on one side of the samples, they were placed on a clean alumina device, which was placed in an oxidation furnace. For depositing 350 nm oxide, the "dry-wet-dry" method was applied at 1000°C. Oxygen flow in the dry oxidation is set at about 2 sccm. In addition, a set of e-beam alignment marks was needed for e-beam lithography steps and transfer of graphene sheet. The Cr electrodes

(20 nm Cr) with W= 30 µm, L= 56 µm and W= 60 µm, L= 56 µm, were fabricated on Sio2 (300 nm)/Si substrate to make aligning markers using conventional macro-Nano processing technologies including photolithography, lift-off process and electron-beam evaporation as shown in figure 1. A large area between the electrodes markers due to locating to part of the graphene sheets created under the electrodes, in order to get a better connection between the electrodes.

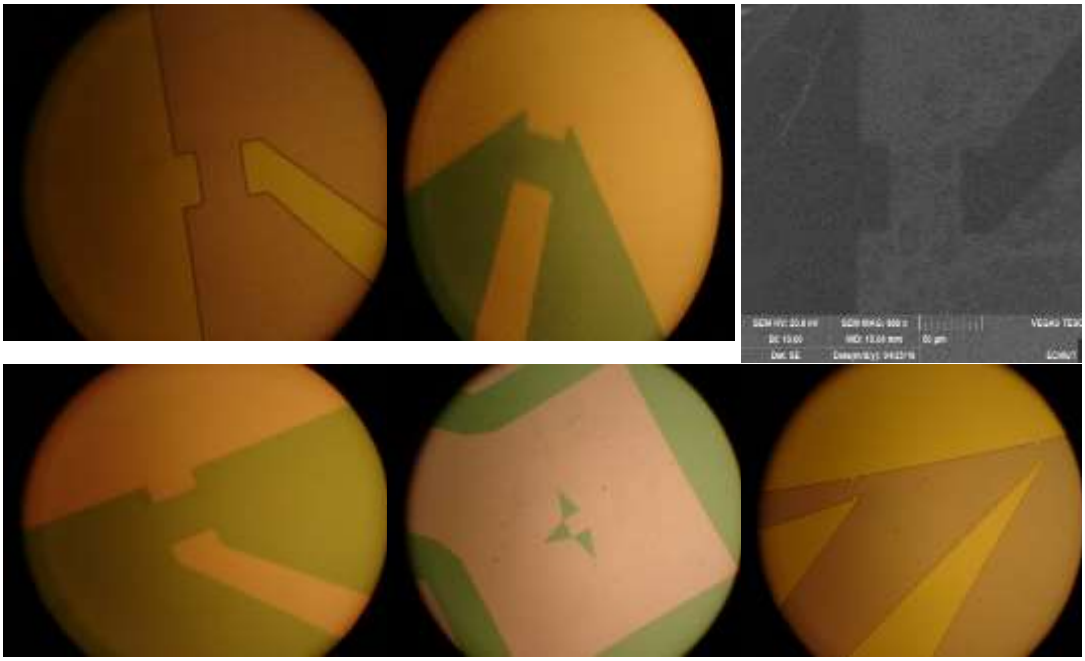


Figure 1. Alignment Maskers Mask, the SEM image and optical microscopy images of the aligning markers electrodes. (Si/Sio2/Cr Markers).

Graphene transfer process

The first step necessary in fabricating devices GFET is to transfer the graphene from the metal Cu substrate onto a device-compatibl substrate. Monolayer Graphene on Cu (10 mm x 10 mm) with thickness (theoretical) 0.345 nm is purchase from Graphenea of Spain. It is crucial to device performance, yield, and uniformity that the quality of the graphene is not degraded during this transfer process. Thus, in an ideal transfer process, the graphene film should remain clean, with no contamination and continuous without folds, cracks, or holes. One

common method for transferring graphene from a transition metal growth substrate is the " PMMA- mediated" approach [5], [6]. In this method a layer of poly (methyl-methacrylate) (PMMA) is coated onto the graphene, and the metal below it is etched away completely by etchant. The PMMA/graphene stack is then transferred onto another substrate, and solvents are used to remove the PMMA and complete the graphene transfer [7]. To transfer the graphene sheet from copper foil on the substrate, the first step is, backside graphene etch by DRIE for 30 Sec at a power of 100 W. Preparation 4% solutions (46 mg/mL) of PMMA in anisole and spin-coating at 4500 rpm for 1 min on a 1.45 × 1.45 cm2 piece of graphene/Cu with thickness 300 nm & bake at 180°C for 1 min. After coating PMMA, the Cu is etched away by iron nitrate; the transparent PMMA/graphene stack usually floats on the solution surface as shown in Figure 2.

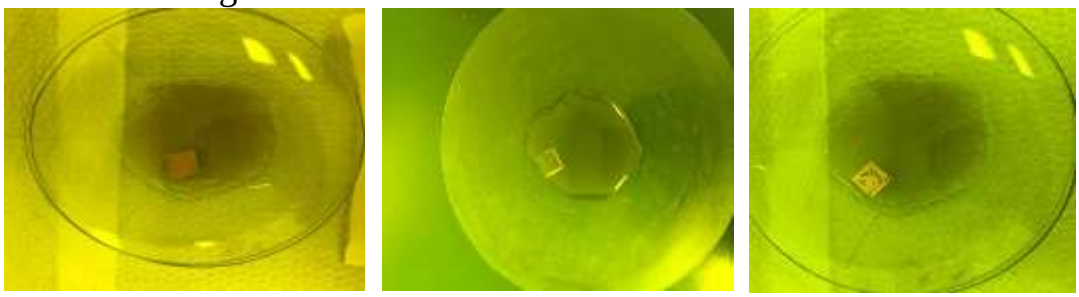


Figure 2. The etching of copper foil, PMMA/graphene stack floats on the solution surface.

After etching of the copper foil graphene/PMMA in distilled water for 10 minutes and rinse it. Then removes ionic and heavy metal atomic contaminants by using a solution of 25:1:1H_2O/H_2O_2/HCl and cleaning the residual metal particles remaining on the PMMA/graphene stack. The PMMA/graphene stack was rinsed by DI water. The next stage is intended for the removal of insoluble organic contaminants with a 25:1:1 $H_2O/H_2O_2/NH_4OH$ solution. To avoid damaging the graphene/PMMA stack in the bubbles created by the H_2O_2, process of washing done at room temperature. After each etching step, the PMMA/graphene stack was rinsed by DI water. To transfer the graphene/PMMA stack, the substrate with piranha solution is activated. Piranha solution (750 micro liters of H2O2 with 250 micro liters of sulfuric acid) increases its hydrophilicity due to an increase in the density of the OH groups on the

Si/SiO2/Cr surface and improves the smoothness of the graphene/PMMA. The increase in the hydrophilicity significantly reduces the formation of large folds and wrinkles, and the PMMA/graphene stack can be transferred without large fold formation onto the target substrate. After the transfer of the graphene/PMMA stack to the substrate, to dry the residual water thoroughly, the sample was baked at 150 ºC for 15 min to evaporate it and improve the contact between the stack and the substrate as shown in Figure 3. PMMA is then removed by solvent rinsing (such as acetone or n-methylpyrrolidinone, (NMP)). Typically after PMMA removal, put the Si/Sio2/graphene in vacuum sputtering with argon gas at a temperature of 300 °C for 20 minutes to be used to further improve the graphene/substrate contact and remove residual particles of PMMA. The end of step of transfer, sample clean with acetone, IPA, DI water, and then dry with low pressure ultra high purity N2.

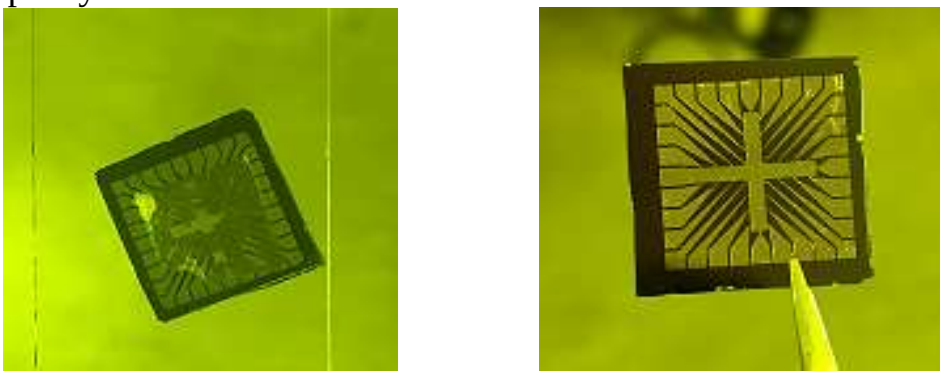


Figure 3. Transfer graphene/PMMA stack on Si/Sio2/Cr markers substrate with water bubbles. Backe the Si/Sio_2/Cr markers/ graphene/PMMA for evaporate water bubbles and improve the contact between the stack and the substrate.

Following this process, a clean and almost crackless graphene film can be transferred to various target substrates.

Raman spectra

Raman spectroscopy is a powerful tool to characterize the structure and defects of carbon materials including carbon nanotubes and graphene. The Z scan is used to focus the laser on the sample surface. The peak position and height of the Raman spectra are known to depend on the

number of layers in graphene [8], [9]. The Raman spectrum, optical image and SEM image of the graphene is shown in figure 4. The spectrum displays the D band and the G band.

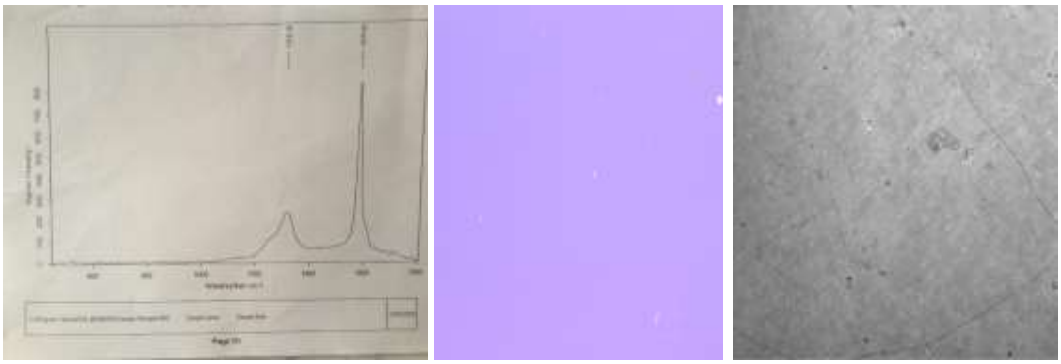


Figure 4. Typical Raman spectra of graphene after Cu etching and transfer graphene sheet onto substrate, and optical microscopy image and SEM image of the graphene.

The transferred graphene film is very clean, with almost no residual particles seen under optical microscope.

Patterning of graphene sheet & Fabrication of electrodes

After graphene has been successfully transferred onto Si/Sio2/Cr Markers substrates, it is ready to be fabricated into electronic devices. The graphene film was first patterned into (60×56) μm2 and (30×56) μm2 stripes by using oxygen plasma for 30 Sec, with power 25w, O_2=25 Sccm, 350 mtorr pressure. Graphene patterning mask with the optical images as shown in Figure 5.

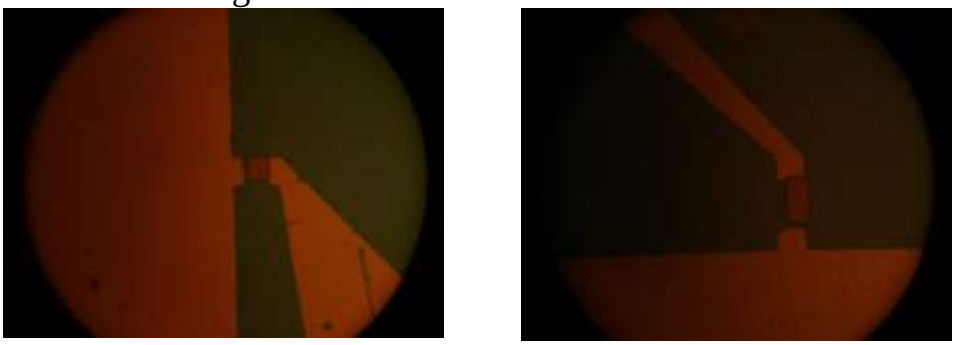


Figure 5. Graphene patterning mask, (Rectangular 60×56 μm2 & 30×56 μm2 with photoresist), to protect graphene in O_2 plasma process.

Metal source/drain contacts were patterned to form FETs with a (60×6) μm^2 and (30×6) μm^2 channel area where the Si-substrate was used as a back gate. Graphene FETs were fabricated (drain-source electrodes 110 nm Au on 30 nm Cr) by standard photolithography processes based on a widely used photoresist, Shipley 1813. After metal deposition, lift-off was performed at 80 °C by soaking the sample in Remover 1165 (1-methyl-2-pyrrolidinone) and then thoroughly rinsed with isopropyl alcohol. An important feature of lift processes is that the side wall profile of the photoresist must be vertical or with an overhang. This causes a break in the deposited metal film and ensures easy lift-off. After normal lithography the side walls are sloping and in order to get an overhang profile the lithographic process is altered slightly. A toluene (formerly chlorobenzene) soak step is included after the UV exposure but before development. The toluene hardens the top layers of the photo resist making them harder to develop away. In general, the exposure time and the development time need to be changed from the optimal conditions to account for the alteration of the resist properties due to the toluene soak. After the expose sample to UV light, immerse the sample in a beaker containing toluene for 1 minute and do not rinse the sample in DI H_2o after the toluene soak. Then now develop the photoresist and the other standard lithography process can be continued. The result of placing the sample in toluene is shown in figure 6.

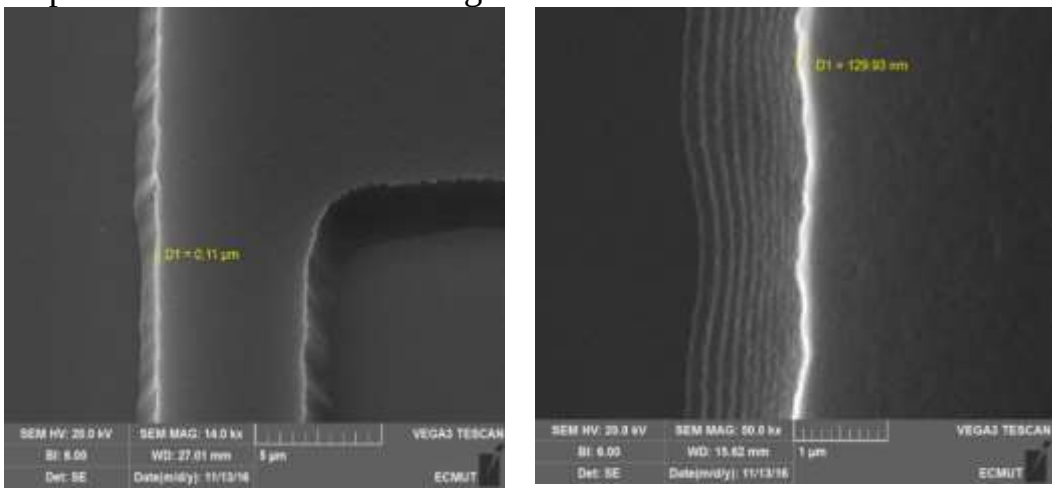


Figure 6. Sample in toluene solution for 2 and 1 minutes.

The mask & optical microscopy images of the source and drain electrodes with SEM images of the GFETs sensor are illustrated in figure 7.

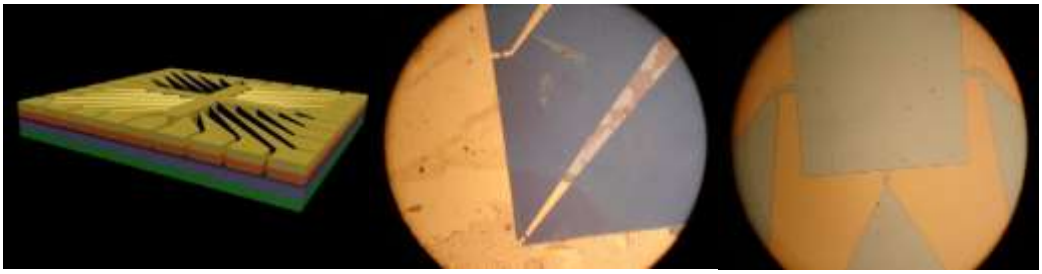


Figure 7. A) The mask of the source and drain electrodes, (31 transistor samples with different dimensions). B) Optical microscopy images of the source/drain contacts.

Transmission Spectrum

Simulation of the Transmission spectrum is done with Atomistix ToolKit (ATK) simulator [10]. Transmission spectrum has a low value in the energy range [-0.5, 1.5] eV, corresponding to the energy window within the band gap of the central semiconducting armchair-edge nanoribbon graphene (Chanel), as shown in figure 8 [10]. The asymmetric position of the electrode Fermi levels relative to the band edges, i.e. the shift of the valence band edge of the central region towards the electrode Fermi levels, is due to the applied gate potential of 1 V.

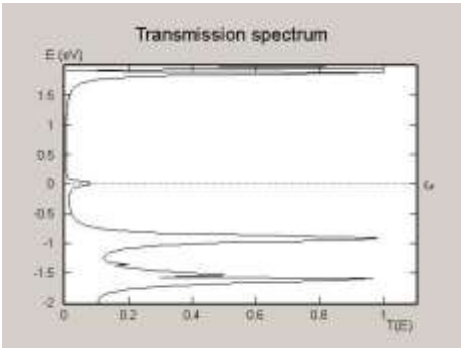


Figure 8. Transmission spectrum of the GRFET with a gate potential of -1 Volt.

In the transistor channel, there are right-moving carriers (electrons with positive velocities) and left-moving carriers (electrons with negative velocities); hence, the net current (I_D) is the difference between the right- and left-moving carriers:

$$I_D = \frac{2e}{h}\int F(E, E_F)\, dE - \frac{2e}{h}\int F(E, E_F - eV_D)\, dE$$

The Fermi energy of the right-moving carriers is controlled by the source potential, while that of the left-moving carriers is controlled by the drain potential. We set the source potential to 0 V for reference and, the same, for a positive drain voltage, E_F at the drain electrode will be correspondingly pulled down. Including the contributions of all the subbands in a semiconducting nanotube, the total drain current becomes the sum of the net current from each subband:

$$I_{D,tot} = \frac{2e}{h}\sum_{j}\int_{E_j - e\emptyset_s}^{\infty} dE\,[F(E, E_F) - F(E, E_F - eV_D)]$$

Where j is the subband index and Ej is the energy minimum or bottom of the jth-subband. The electron current Ie can be expressed by following the Landauer–Büttiker formalism.

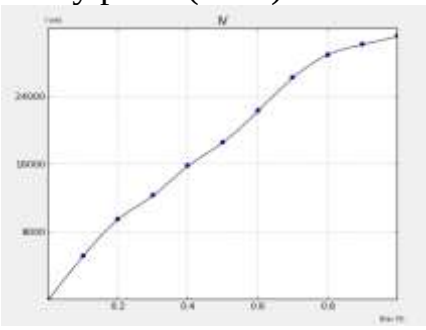
$$I_e = \frac{4e}{h}\int_{E_{cb} - e\emptyset_s}^{\infty} [T_{sd}(E)F(E, E_F) - T_{ds}(E)F(E, E_F - eV_d)]\, dE$$

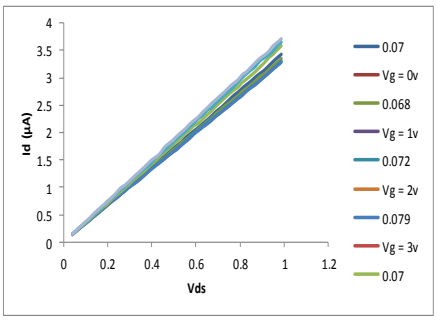
Where Tsd is the source to drain transmission probability or coefficient of an electron-wave propagating from the source to the drain, successfully through both Schottky barriers, and vice versa for Tds. The total drain current is ID = Ie + Ih.

Results

Bandgap tenability is beneficial to transfer graphene characteristic from metal to semi-conductive properties. And current–voltage characteristics of graphene transistors indicate the ambipolarity of graphene. Bipolar property in GFET structure means the passing of current by electrons in a range of gate voltage and by holes in another range of gate voltage [11]. Dirac point means zero concentration of carriers when the field is zero. In an ideal case, the transfer characteristic of GFET should be quasi ballistic. Through utilization of bipolar gate voltage, the carriers in graphene transform electrons (holes) from holes (electrons)

continuously. Negative gate voltage makes holes conductive in graphene. Otherwise, electrons are dominant in graphene under positive gate voltage. So resistance or conductivity of graphene device changes with the variable gate voltage. Leakage current between the channel and gate is a critical factor for device reliability when making graphene gate controlled electronic devices, and more researchers are devoted to diminishing the leakage current. The GFET exhibits very small leakage current between the channel and gate due to the channel and the gate dielectric material being separated by an ultrathin blocked graphene connection in the FET device. To investigate the electrical properties of the GFETs device, the output and transfer characteristics of the GFETs sensor were obtained. Electrical properties of the GFET were measured by using an Agilent 4145B semiconductor parameter analyzer. Figure 9 show electrical measurement results for a typical GFET. Figure 9a shows the drain current, Id as a function of the drain voltage, Vd, measured at various gate voltages for Vd sweeping ranges. The drain-source current decreases with a slight reduction of the gate voltage, indicating that the device reaction is sensitive to the gate voltage. All curves overlap, indicating that the contact between the source/drain metal and graphene is very stable. Figure 9b is field effect measurement results. The transfer characteristic curve (Id as a function of back gate voltage, Vg) is smooth with little hysteresis, and the conductivity minimum associated with the Dirac point is near 1 V. Dirac point, which can be identified as the charge neutrality point (CNP).





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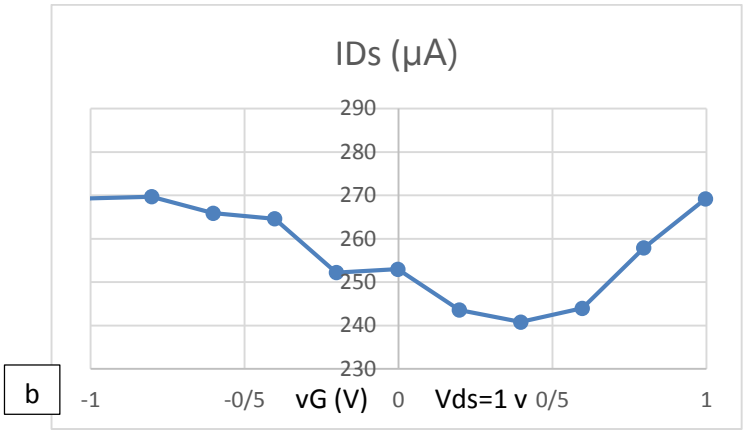

Figure 9. Electrical properties of a GFET. a) Id-Vd curves measured at various Vg with Vd sweeping ranges. b) Typical V-shape bipolar property output.

These results indicate that the surface contamination due to the graphene transfer process is very low; therefore, the device performance is repeatable without any annealing treatment (thermal or current) needed. The gate leakage current was in the nA range for all measurements.

Conclusion

In summary, we have studied clean methods for transferring graphene from Cu substrates to target substrates and fabricated the GFET based on graphene. The graphene/wafer-substrate interface resulting from this clean transfer process is greatly improved. Lab results shows that the number of cracks in transferred graphene films can be reduced by controlling the hydrophilicity of the target substrate and baking. Graphene as the conducting material shows the obvious ambipolar characteristics at a small range of gate voltage on the back-gated FET devices under ambient conditions, and the devices are highly responsive to the low gate voltage. Design and manufacture of explosives detector sensors based on GFETs with biological receptor that capable of responding to several different types of explosives in real time, is the next thing the research group will publish in this journal.

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